UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,178	04/07/2004	Sandeep Brahmadathan	POU920040034US1	7369

46369 7590 03/12/2007

HESLIN ROTHENBERG FARLEY & MESITI P.C.
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER	
TORRES, JOSEPH D	
ART UNIT	PAPER NUMBER
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,178	BRAHMADATHAN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-11,18-22,24 and 31-35* is/are allowed.

6)☒ Claim(s) *1-6,12-17,23 and 25-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/07/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "606", "607" and "608" in Figure 6. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 12-17 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor, Richard D. et al. (US 20030131277 A1, hereafter referred to as Taylor).

35 U.S.C. 102(e) rejection of claims 1, 12 and 23.

Taylor teaches testing addressed data and associated control information of a memory device for error (the <DATA PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information), wherein the addressed data is to be provided responsive to a request (page 2, paragraph [0017] in Taylor) therefor; and automatically retrieving contents of an addressed storage compartment of a second memory device if error is detected by the testing, and providing the contents of the addressed storage compartment responsive to the request (paragraph [0018], second column on page 2 in Taylor), wherein the memory device and the second memory device comprise separate memory devices (Cache memory is a first memory device and system memory is a second memory device in Figure 2 of Taylor).

35 U.S.C. 102(e) rejection of claims 2 and 13.

CPU 12 in Figure 2 of Taylor receives requested data over System Bus 14 regardless of where the data comes from; algorithm for automatic retrieving is transparent to the CPU.

35 U.S.C. 102(e) rejection of claims 3 and 14.

Figure 2 in Taylor.

35 U.S.C. 102(e) rejection of claims 4 and 15.

Steps 100 and 110 in Figure 3 of Taylor.

35 U.S.C. 102(e) rejection of claims 5 and 16.

The <DATA PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information.

35 U.S.C. 102(e) rejection of claims 6 and 17.

The <DATA PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information.

A parity code is an error detecting code. A parity code is capable of detecting at least twice as many errors as it is capable of detecting.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 25-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor, Richard D. et al. (US 20030131277 A1, hereafter referred to as Taylor).

35 U.S.C. 103(a) rejection of claim 25.

Taylor teaches testing addressed data and associated control information of a memory device for error (the <DATA PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information), wherein the addressed data is to be provided responsive to a request (page 2, paragraph [0017] in Taylor) therefor; and automatically retrieving contents of an addressed storage compartment of a second memory device if error is detected by the testing, and providing the contents of the addressed storage compartment

responsive to the request (paragraph [0018], second column on page 2 in Taylor), wherein the memory device and the second memory device comprise separate memory devices (Cache memory is a first memory device and system memory is a second memory device in Figure 2 of Taylor).

However Taylor does not explicitly teach the specific use of computer program instructions for implementing the method recited in claim 25.

The Examiner asserts that computer programs provide a flexible and scalable means for implementing a method.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Taylor by including use of computer program instructions for implementing the method recited in claim 25. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of computer program instructions for implementing the method recited in claim 25 would have provided a flexible and scalable means for implementing \the method recited in claim 25.

35 U.S.C. 103(a) rejection of claim 26.

CPU 12 in Figure 2 of Taylor receives requested data over System Bus 14 regardless of where the data comes from; algorithm for automatic retrieving is transparent to the CPU.

35 U.S.C. 103(a) rejection of claim 27.

Figure 2 in Taylor.

35 U.S.C. 103(a) rejection of claim 28.

Steps 100 and 110 in Figure 3 of Taylor.

35 U.S.C. 103(a) rejection of claim 29.

The <DATA PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information.

35 U.S.C. 103(a) rejection of claim 30.

The <DATA PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information.
A parity code is an error detecting code. A parity code is capable of detecting at least twice as many errors as it is capable of detecting.

Allowable Subject Matter

4. Claims 7-11, 18-22, 24 and 31-35 are allowed.

The following is an examiner's statement of reasons for allowance:

Taylor (US 20030131277 A1, hereafter referred to as Taylor) teaches testing addressed data and associated control information of a memory device for error (the <DATA

PARITY GOOD?> step in Figure 3 is a test for addressed data; the <TAG PARITY GOOD?> step in Figure 3 is a test for associated control information), wherein the addressed data is to be provided responsive to a request (page 2, paragraph [0017] in Taylor) therefor; and automatically retrieving contents of an addressed storage compartment of a second memory device if error is detected by the testing, and providing the contents of the addressed storage compartment responsive to the request (paragraph [0018], second column on page 2 in Taylor), wherein the memory device and the second memory device comprise separate memory devices (Cache memory is a first memory device and system memory is a second memory device in Figure 2 of Taylor).

However the prior art of record are not concerned with and do not teach, suggest, or otherwise render obvious the following feature found in claim 7: "ascertaining from a change bit of the associated control information whether the addressed data has changed since contents of an addressed storage compartment of a second memory device were written to the memory device as the addressed data, wherein the memory device and the second memory device comprise separate memory devices". Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 7.

Claims 18, 24 and 31 recite substantially the same features as in claim 7.

Claims 8-11, 19-22 and 32-35 depend form claims 7, 18 and 31.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JOSEPH D. TORRES
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133